A 18 mW Triple 2 GHz CMOS PLL for 3G Mobile Systems with −113 dBc/Hz GSM in-band Phase Noise and Dual-Port GMSK Modulation

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Abstract — **A PLL for 3G systems achieves −113-dBc/Hz close-in phase noise in the GSM Band and consumes 18mW (2mA for the 5V charge-pump and 4mA under 1.875 Volts for the remaining blocks). The GMSK Dual-Port modulation system achieves 1.2° rms phase error and a noise level of −67dBc at 400 kHz offset from carrier in a 30kHz BW. Three PLLs are integrated on the same die and are synchronized to avoid crosstalk issues.**

I. Introduction

Third generation (3G) mobile systems cover multiple standards that require an advanced integration of radio components. The need for frequency synthesizers is tripled compared to a 2G radio transceiver. Power consumption of these PLLs becomes even more critical to maintain battery life, while pursuing improved phase noise performances. In this work, three CMOS PLLs are integrated on the same die and achieve −113 dBc/Hz GSM in-band phase noise while consuming 18mW. Furthermore, the use of direct GMSK modulation goes toward higher integration and lower drain current.

II. Circuit Architecture

The schematic of the 3-PLLs chip is shown in Figure 1.

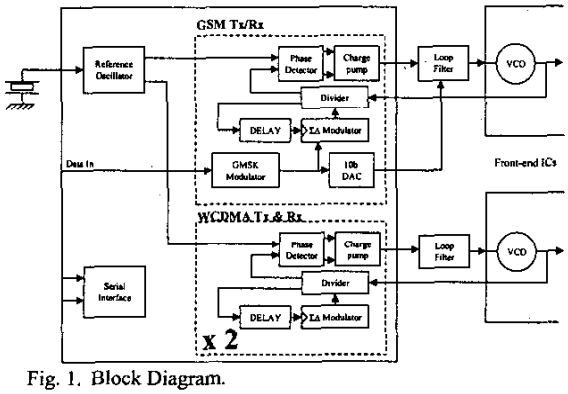

Fig. 1. Block Diagram.

One PLL is intended for the GSM Tx and Rx paths, while the 2 others provide the frequency generation of the WCDMA Tx and Rx standard. They all use an unique 26MHz reference crystal oscillator. The digital core contains the 3[rd] order ΣΔ fractional-N modulators, the GMSK modulator for the GSM Tx path and the serial programming interface. The loop filters are external and the VCOs are integrated in the front-end ICs.

III. Circuit Design

Requirements for lock time and phase noise are stringent, especially in GSM mode [1]. Widening the loop filter bandwidth reduces the lock time and improves the PLL immunity to external disturbances, but increases the out-of-band noise. Lowering the PLL in-band phase noise is key as one can increase the loop bandwidth while meeting the out-of-band critical noise specifications.

High frequency dividers can be properly designed to minimize their jitter. The use of a high Q resonator (Crystal) is sufficient to provide a clean reference of less than −150 dBc/Hz @ 1kHz offset from carrier. Generally, the charge-pump remains the main close-in phase noise contributor.

A. Charge-Pump.

The charge-pump is implemented in a conventional tri-state structure with a trickle current source to avoid the phase detector dead-zone [6]. In locked conditions, the down pulse compensates for the constant trickle current, and no up pulse occurs. The duty cycle δ is equal to the ratio between the trickle current I_{tr} and the charge-pump gain I_{cp} (down pulsed current). The charge-pump schematic is shown in figure 2. M4 is the trickle current source, M3 is the down-pulsed current source, and M1-M2-M5 compose the switching circuitry. M5 forces the gate voltage of M3 to ground to speed up the switching. The up pulse circuitry is not represented.

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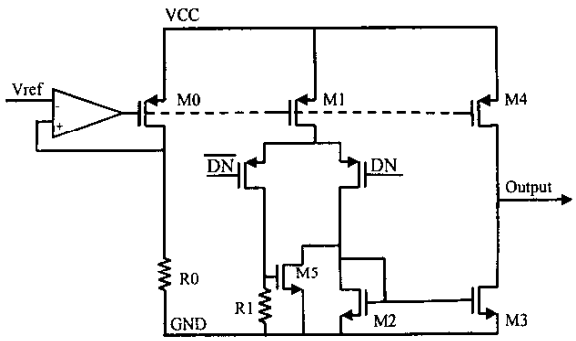


Fig. 2. Charge-Pump simplified schematic.

A detailed noise analysis shows that the biasing circuit is a second-order contributor. It acts as a common mode signal to the trickle and down current sources, and thus cancels out at the charge-pump output in locked conditions. This allows a dramatic power saving in the biasing circuitry. Furthermore, the charge-pump noise contribution is closely related to its Signal to Noise Ratio (SNR): to a given power consumption corresponds a noise limit that cannot be overcome. This limit derives from the contributions of devices M1, M2, M3, M4. Let α be the ratio between the current flowing through M1-M2 and the charge-pump gain. Let Vd_{sat} be the saturation voltage of M1, M2, M3 and M4 fixed by the output voltage compliance (VCO input range). The theoretical analysis leads to the following relationship between output phase noise due to the charge-pump L_{SSB} and the charge-pump drain current I_{total}:

$$L_{SSB} = 10 \cdot \log\left[2(\pi N)^2 \frac{32kT}{3V_{dsat}} \frac{\delta(1+\alpha)\left(\delta + 1/\alpha\right)}{I_{total}} \right] \quad (1)$$

Where N is the division ratio. I_{total} only accounts for the output stages consumption and not for the biasing and switching circuitry.

For a given I_{total}, the noise is found to be minimal when $\delta(1+\alpha)(\delta+1/\alpha)$ is minimal. The variable δ must be high enough to ensure charge-pump linearity in fractional-N mode. Low values lead to a highly non-linear charge-pump and high values generate too much thermal noise. Usually values between 1/6th and 1/3rd provide good compromise between linearity, noise and power consumption. The optimum values of α are then derived from the values of δ:

$$\begin{aligned} \delta = 1/3 &\Rightarrow \alpha \approx 1.73 \\ \delta = 1/6 &\Rightarrow \alpha \approx 2.50 \end{aligned} \quad (2)$$

For our application where the trickle current is selectable between 1/6th and 1/3th, an α of 2 is chosen.

Therefore, the main trade-off results in the choice of the charge-pump gain. Increasing I_{cp} decreases the phase noise at the expense of drain current. Three different charge-pump gains were simulated using a periodic steady-state approach. The resulting power consumption and phase noise contribution are plotted on Figure 3. It shows a good matching between equation (1) and simulations data.

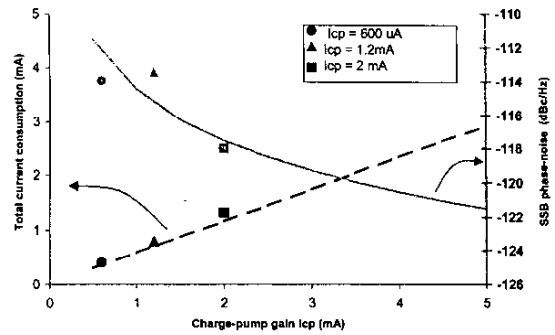


Fig. 3. Noise and Consumption tradeoff.

Note that the charge-pump gain current I_{cp} strongly impacts loop performances (closed-loop gain), reducing its range of optimization. For the Tx GSM charge-pump design, the gain I_{cp} is 2mA. The simulated charge-pump noise floor is –118 dBc/Hz, within 2dB from the theoretical limit, mostly due to the additional switching noise.

B. Design for High Linearity.

Linearity of the PLL transfer function is another critical parameter in the design as the fractional-N modulation is activated. In the charge-pump, non-ideal edges of the current pulse create a non-linear relationship between the phase error and the injected charge, generating an additional noise source. An original methodology was developed to evaluate the impact of the charge-pump non-linearity on the output phase noise. The charge-pump non-linearity is modeled as an additional noise source that is processed by the linear model of the PLL. The charge-pump has been designed in such a way that non-linearities yield to a noise floor of –130dBc/Hz, well below thermal noise. Figure 4 shows the 3rd order $\Sigma\Delta$ noise shaping in both ideal and non-linear cases. Figure 5 displays the impact on the output phase noise.

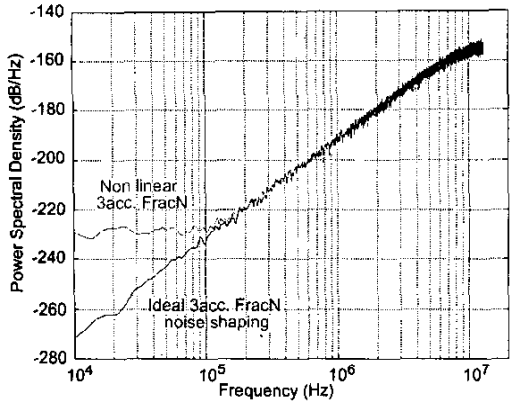


Fig. 4. 3rd Order ΣΔ noise shaping at charge-pump output

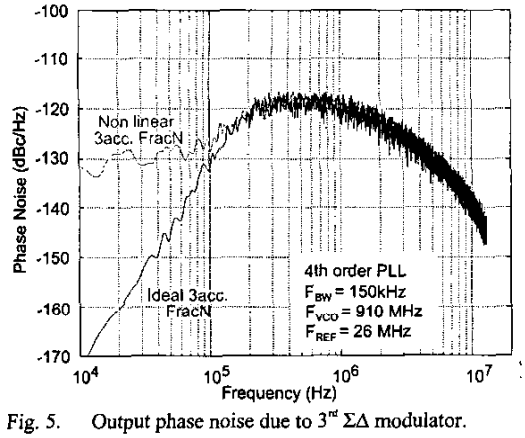


Fig. 5. Output phase noise due to 3rd ΣΔ modulator.

An outstanding measured in-band phase noise of −113 dBc/Hz in 3rd order ΣΔ fractional-N mode is achieved in GSM band, with a 26 MHz reference clock, as shown in Figure 6.

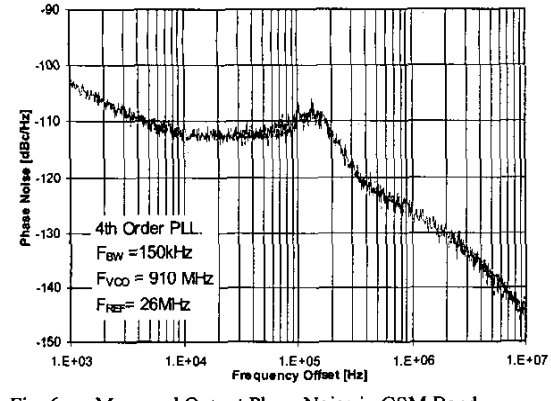


Fig. 6. Measured Output Phase Noise in GSM Band.

At -113dBc/Hz, the dominant contributor is the charge-pump as expected, but some other noise sources (crystal oscillator buffers) are no more negligible. Besides, only 1dB degradation between integer and fractional-N mode is measured, showing that the charge-pump is sufficiently linear.

C. GMSK Modulation scheme.

Below a given in-band noise level, the fractional-N ΣΔ shaped noise becomes dominant and thus prevents a further increase of the bandwidth. In this case, direct GMSK modulation through the fractional-N modulator is not viable as the modulation mask exceeds the loop bandwidth. To compensate for the limited bandwidth of the main modulation path, a 10 bit ΣΔ DAC is connected to the external passive loop filter (Figure 1), providing the high frequency part of the modulation. With a 150kHz loop bandwidth, this Dual-Port system achieves a GMSK phase error of 1.2° rms and meets the 400 kHz offset from carrier GSM noise specification with 7 dB margin, as shown in Figure 7.

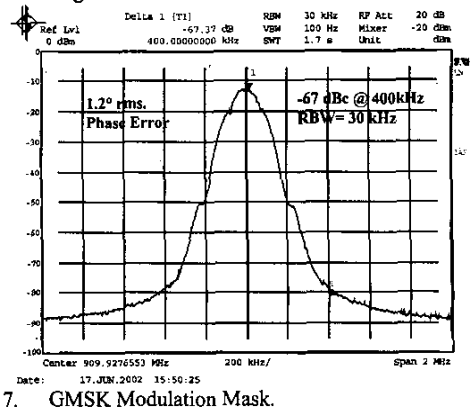


Fig. 7. GMSK Modulation Mask.

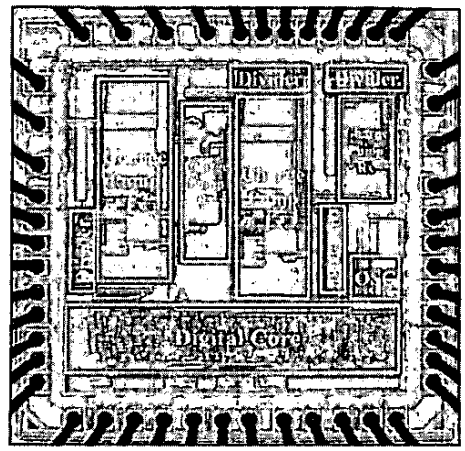
D. PLLs synchronization.

In 3G systems, GSM and WCDMA transfers can occur simultaneously. To avoid crosstalk between PLLs, time-sharing technique is used. Each PLL is active during a given timeslot within the reference period. The digital activity is also separated from the analog activity to avoid analog circuitry from being polluted by digital noise. The reference period is thus divided in 4 slots: 3 for the PLLs, and the last one for the digital core. As the fractional-N modulator is clocked by the output of the feedback divider, one must ensure that it will not interfere with the activity of the phase detector and the charge-pump. Programmable delays are thus inserted between the output of the divider and the input of the modulator as in figure 1. When the delays are not precisely selected, up to 15 dB phase noise degradation is observed, both in the considered PLL and in

the 2 others. However, selecting the adequate delays allow to run the 3 PLLs together without significant phase noise degradation (less than 1dB). Layout was also done to isolate the digital core from the rest of the chip. The digital core is in an isolated N well and is surrounded by large P+ guard rings.

IV. Performance Summary

Figure 8 shows the picture of the IC that is processed in a standard 0.18µm CMOS process and occupies 2.4 mm².



The power consumption for one PLL is 18 mW (including phase detector, charge-pump, divider and modulator and excluding the VCO) and mainly comes from the charge-pump (10mW), because of its 5 Volt supply to accommodate for the VCO tuning range.

TABLE I
PERFORMANCE SUMMARY

Operating bands	GSM / DCS / PCS / WCDMA
Technology	0.18 µm CMOS
Chip area	2.4 mm²
Power consumption (One PLL)	18 mW
In-band phase noise (900 MHz, Fref=26MHz)	-113dBc/Hz
Lock time (150kHz BW)	50 µs
GMSK Phase Error	1.2° rms.
GMSK Modulation Mask (RBW=30kHz)	-67 dBc @400 kHz

Figure 9 displays some previously published CMOS design performances. All in-band phase noise results were scaled to a division ratio of 35 for comparison purposes. Power consumption excludes VCO and loop filter. The in-band phase noise for this given power consumption is the lowest ever published [2] [3] [4] [5].

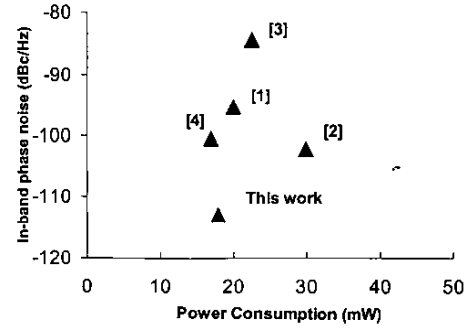


Fig. 9. Phase noise and power consumption comparison.

V. Conclusion

A low power low noise triple PLLs chip has been developed for 3G applications. Very low in-band phase noise is reached by means of a theoretical charge-pump noise analysis, and through an original methodology to predict phase noise due to non-linearities in fractional mode.

Acknowledgement

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References

[1] : 3GPP specifications TSG/GERAN/WG1 05.05 "Radio Aspects".

[2] : J. Craninckx and M. Steyaert, « A Fully Integrated CMOS DCS-1800 Frequency Synthesizer, Proceedings of the ISSCC, 1998.

[3] : Woogeun Rhee, Akbar Ali, Bang-Sup Song, "A 1.1 GHz CMOS Fractional-N Frequency Synthesizer with a 3b 3rd-Order ΣΔ Modulator", Proceedings of the ISSCC, 2000.

[4] : Rami Ahola and Kari Halonen, "A 2GHz ΣΔ Fractional-N Frequency Synthesizer in 0.35µm CMOS", Proceedings of the ESSCIRC, 2000.

[5]: Sang Oh Lee, "A 17mW, 2.5GHz Fractional-N Frequency Synthesizer for CDMA-2000", Proceedings of the ESSCIRC, 2001.

[6]: Alexander W. Hietala, David M. Gonzalez, Patent US 6,327,319B1 "Phase Detector with Frequency Steering".